INVESTIGATION AND APPLICATION TO LNA OF AN InP-HEMT OPERATED AT ULTRA LOW DC POWER LEVELS

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Abstract

The noise and gain for an InP HEMT were investigated as a function of DC power consumption. A special chip carrier in mixed coplanar waveguide/microstrip technology was developed for easy handling of the chip and to minimize the mounting parasitics. A complete S parameter and noise parameter model for the transistor and the carrier have been extracted. Measurements of the transistor mounted on the carrier gave an associated gain of 10 dB and noise figure lower than 0.7 dB at a DC power level of 200 µW at 10 GHz. An X band one-stage amplifier with low DC consumption based on this transistor was built. The amplifier had a gain of 8-10 dB for the frequency range 8-12 GHz at $V_{ds} = 0.35\,V$, $I_{ds} = 3.9\,mA$. The noise figure of the complete amplifier was measured to 1.6 dB at 10 GHz. The HEMT was manufactured in our own laboratory process.

Introduction

Low DC-power consumption is an important parameter in many amplifier applications for example in satellite receivers and mobile telephony. It is desirable to minimize the power consumption to the lowest possible level and simultaneously maintaining high gain and low noise performance.

InP HEMT

The suitable transistor for low power consumption is a HEMT based on InP, known for its excellent noise characteristics and high gain. The perspective view of the transistors layers is shown in Fig. 1.

This InP based transistor was developed at Chalmers University of Technology, [1].

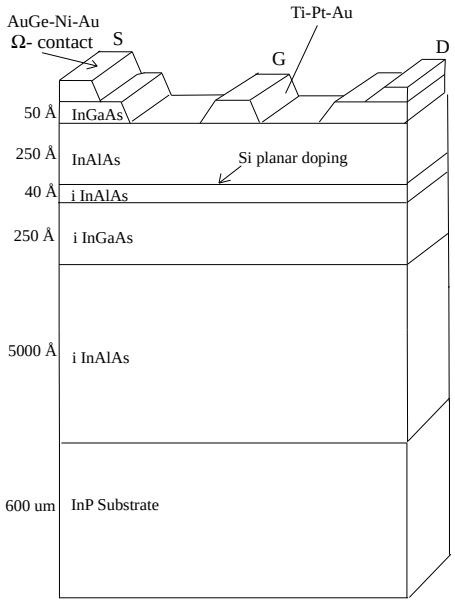

Fig. 1. InP based HEMT.

The dimensions of the chip are 225x400x125 µm and it has a gate length of 0.15 µm and a gate width of 2x50 µm.

Chip carrier

Packaging the chip in a standard package will increase the parasitics and lower the performance of the transistor. A special coplanar waveguide/microstrip fixture with very low parasitics was developed, Fig. 2. The fixture was manufactured in alumina.

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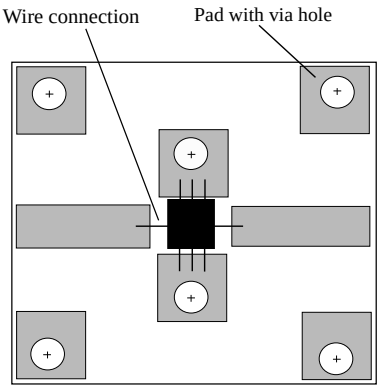

Fig. 2. Top view of the chip carrier

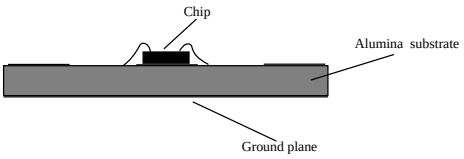

Fig. 3. Side view of the chip carrier.

The transistor was mounted on a fixture with non-conductive epoxy. The overall substrate size is 2600x2255 µm with a via hole diameter of 254 µm. All lines are 50 Ω. The substrate is 254 µm thick alumina with ε_r=9.9 and all lines, pads and the ground plane consist of 300 Å thick TiW with 3.5-5 µm thick Au layer. The chip carrier has footprints at the input and output for probing with coplanar probes. The chip carrier was then permanently fixed on a removable brass carrier, Fig. 4.

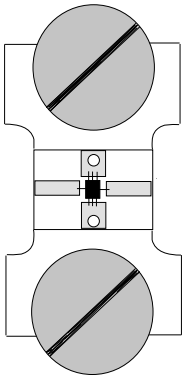

Fig. 4. Chip carrier mounted on a brass carrier.

The carrier in Fig. 2 was used for S parameter and noise characterization in a probe station. The chip carrier in Fig. 4 has only microstrip lines. It was used in the design of the LNA. The simulations in Momentum, from HP, showed that the differences between the two carriers were negligible.

Modeling of InP HEMT

The transistors equivalent circuit was extracted from the measured S parameters. The extraction was done by an in house developed parameter extractor, [2]. The equivalent circuit of the transistor is shown in Fig. 5.

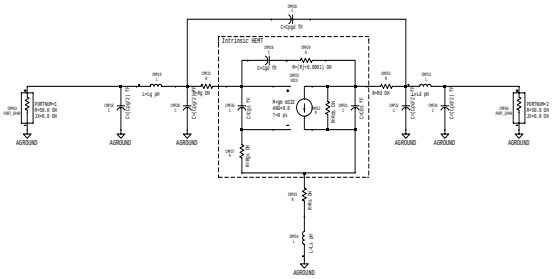

Fig. 5. Equivalent circuit for a HEMT.

The equivalent circuit is not frequency dependent but bias dependent, therefore a set of model parameters has been extracted for every bias point. The so called intrinsic parameters inside the dashed square change when the bias point is altered. The other parameters of the equivalent circuit are called parasitics and they are bias independent.

We have obtained an excellent agreement between the simulated and measured S parameters.

In order to have a complete model of the transistor also the noise parameters, i.e. R_n, F_{min} and Γ_0 have to be measured and simulated. The Pospieszalski [3] noise model has been used i.e. all the resistors in the equivalent circuit except for R_{gs} and R_{ds} have an equivalent noise temperature equal to the ambient temperature, in this case T_a=300 K. T_g and T_d is the equivalent noise temperature of R_{gs} and R_{ds} respectively. T_g and T_d have then been changed until the noise model fits the measured noise parameters, by using optimi-

zation in the MDS. Fig. 6 below shows the extracted values of T_g and T_d for different bias points at T_a=300K.

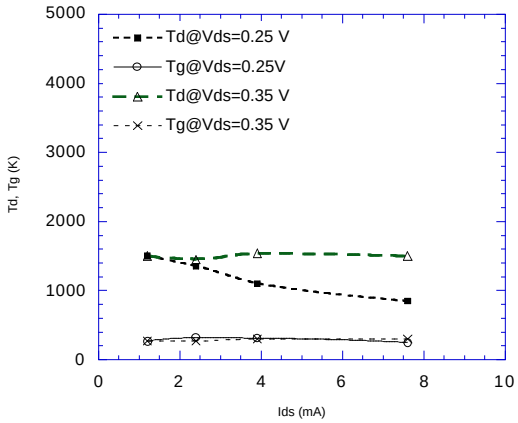

Fig. 6. Extracted Td and Tg versus Ids and Vds.

The measured and simulated noise parameters showed good agreement for the frequency range of 2-26 GHz.

Carrier modeling

The chip mounted in the carrier was simulated in MDS. Using the available models for via holes and bonding wires we have obtained a very good agreement between the measurements and simulations. Typical measured and simulated results for S_{11} and S_{21} are shown in Fig. 7 a-b.

The equivalent circuit for the carrier mounted chip is shown in Fig. 8.

Also the noise parameters were measured and simulated with good agreement.

All modeling was done at the bias point V_{ds}=0.35 V, V_{gs}=-0.4 V, I_{ds}=3.9 mA. The TRL calibration procedure was used in the measurements.

Amplifier design

An LNA was designed with the InP14 HEMT. Fig. 9 shows the noise figure and gain as a function of DC power level at 300 K.

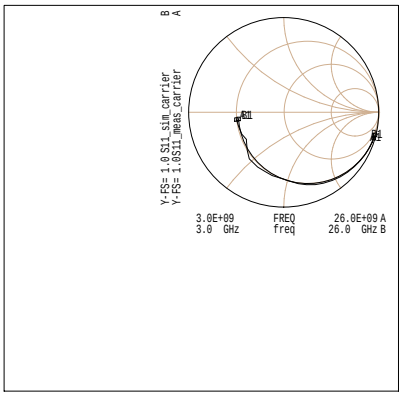

Fig. 7 a. S_{11} measured and simulated on the carrier.

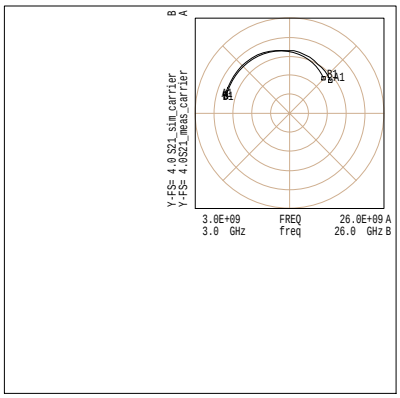

Fig. 7 b. S_{21} measured and simulated on the carrier.

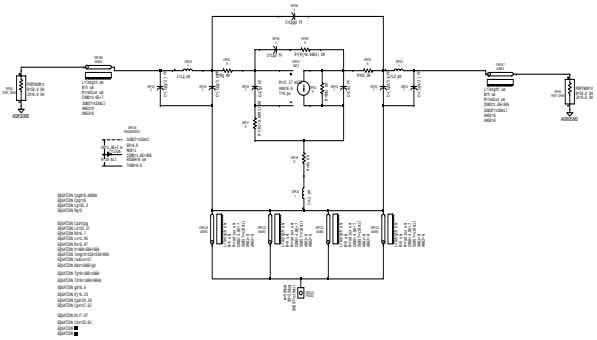

Fig. 8. Equivalent circuit for the carrier mounted chip including bonding wires and via holes.

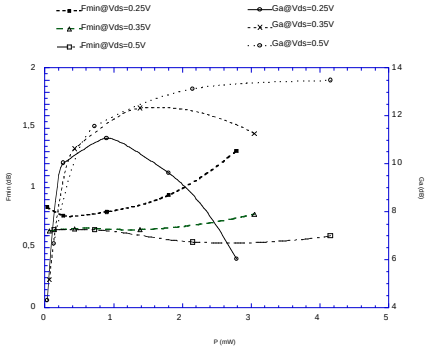

Fig. 9. Measured F_{min} and G_a as a function of DC power for InP14 at 10 GHz and 300K.

The bias point of $V_{ds} = 0.35V$ and $I_{ds} = 3.9mA$ offers a good compromise for low noise, high gain and stability of the amplifier.

The measured and simulated results for the LNA are shown in Figs. 10-13.

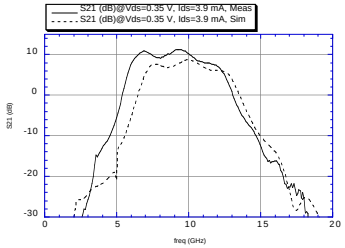

Fig. 10. Measured and simulated S_{21}.

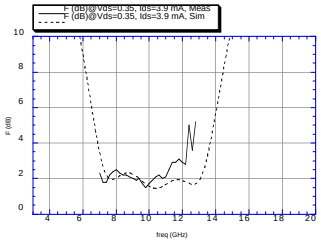

Fig. 11. Measured and simulated noise factor.

Conclusions

We have successfully modeled an InP HEMT at ultra low power bias and used it in a single stage LNA. The amplifier had a gain of 8-10 dB for the frequency range 8-12 GHz at $V_{ds} = 0.35$ V, $I_{ds} = 3.9$ mA. The noise figure was measured to 1.6 dB at 10 GHz.

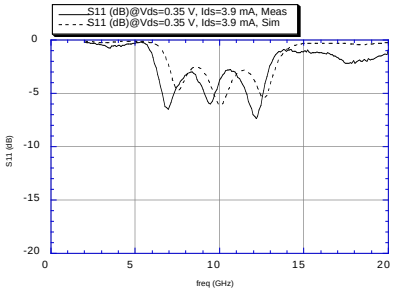

Fig 12. Measured and simulated S_{11}.

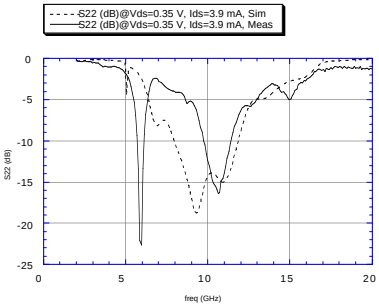

Fig. 13. Measured and simulated S_{22}.

The alumina carrier and brass fixture were very practical in handling fragile chips with excellent RF performance. The investigated InP14 HEMT is a very interesting alternative for LNA when ultra low DC power levels are required.

Acknowledgments

This work was partly supported by Anders Emrich from Omnisys AB, Gothenburg, Sweden. We also kindly acknowledge support from Gunnar Eriksson, Swedish Defense Material Administartion.

References

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[2] Mikael Garcia, "Small-Signal, Large-Signal and Noise Modeling of HEMTs", Technical Report No. 202L, Chalmers University of Technology, 1995.

[3] Marian W. Pospieszalski, "Modeling of Noise Parameters of MESFET´s and MODFET´s and Their Frequency and Temperature Dependence", IEEE Transactions on Microwave Theory and Techniques, Vol. 37, No. 9, 1989.